

**National University of Computer and Emerging sciences**

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| **Course: Computer Logic and Design Lab** | **Lab Instructor: Muhammad Farrukh** |  |
| **Course Instructor: Ms Nazish Saleem Abbas** | **Lab 5** |
| **Section:J2** | **Total Marks:30** |

**Objectives:**

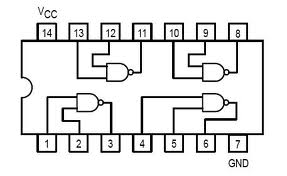
* To learn and understand the working of NAND gate and NOR gate
* SOP expressions from K-map

**Introduction to NAND Gate**

74LS00 IC contains four 2-input NAND gates. The function table and connection diagram for this IC are shown below:

**Function Table Connection Diagram:**

|  |  |  |
| --- | --- | --- |
| **Inputs** | | **Output** |
| **A** | **B** | **Y** |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |



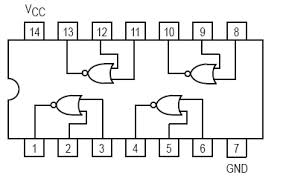
H= Logic High, L= Logic Low

**Introduction to NOR Gate**

74LS02 IC contains four 2-input NOR gates. The function table and connection diagram for this IC are shown below:

**Function Table: Connection Diagram:**

|  |  |  |
| --- | --- | --- |
| **Inputs** | | **Output** |
| **A** | **B** | **Y** |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |



H= Logic High, L= Logic Low

**NOR and NAND Implementation on logic trainer:**

**Question#1: Implement the AND and OR gate using only the NAND gates**

1. **Z=A.B b. X=A+B c. XOR Gate**

**Question#2: Implement the AND and OR gate using only the NOR gates**

1. **Z=A.B b. X=A+B c. XNOR Gate**

**Question # 3:** For the Boolean function do the following:

1. Find truth table
2. Find minimal SOP expression for Boolean function using K-map. Draw K-map in the space given below. Implement it on logic trainer.